What is claimed is:

1. A semiconductor integrated-circuit device, comprising:

a plurality of flip-flop circuits for acquiring and holding signals by use of clock signals; and

a plurality of signal transferring paths each including a plurality of CMOS-constructed logic gate circuits provided between one pair of flip-flop circuits within said plurality of flip-flop circuits;

said plurality of signal transferring paths further including:

a first signal transferring path in which said plurality of logic gate circuits are constituted by enhancement-type MOSFETs, said first signal transferring path providing a signal transferring delay time equal to, or less than, a permissible signal transferring delay time; and

a second signal transferring path in which, among all said plurality of logic gate circuits, a logic gate circuit having a delay time longer than said permissible signal transferring delay time when the logic gate circuit is constituted by an enhancement-type MOSFET is replaced with a depletion-type MOSFET so that the second signal transferring path may provide a signal transferring delay

time equal to, or less than, said permissible signal transferring delay time.

2. The semiconductor integrated-circuit device according to claim 1, wherein the depletion-type MOSFET constituting the logic gate circuit to be replaced is formed by applying a manufacturing step for depletion to a MOSFET having the same pattern and size as those of the enhancement-type MOSFET that has not been replaced.

3. The semiconductor integrated-circuit device according to claim 1, comprising:

enhancement-type MOSFETs with high threshold voltage, enhancement-type MOSFETs with low threshold voltage, and depletion-type MOSFETs;

wherein said flip-flop circuits and said first signal transferring path are constituted by said enhancement-type MOSFETs with high threshold voltage; and

wherein said second signal transferring path is constituted by said enhancement-type MOSFETs with high threshold voltage and said enhancement-type MOSFETs with low threshold voltage, by said enhancement-type MOSFETs with low threshold voltage, by said enhancement-type MOSFETs with low threshold voltage and said depletion-type MOSFETs, or by said depletion-type MOSFETs.

4. The semiconductor integrated-circuit device according to claim 3, further comprising MOSFETs with high

withstand voltage and high threshold voltage, wherein input/output circuits for exchanging signals with external terminals are constituted by said MOSFETs with high withstand voltage and high threshold voltage, and said MOSFETs with high threshold voltage.

5. The semiconductor integrated-circuit device according to claim 3, further comprising a memory circuit, wherein a memory array in said memory circuit is constituted by said enhancement-type MOSFETs with high threshold voltage, and a peripheral circuit of this memory array is constituted by said enhancement-type MOSFETs with low threshold voltage.

6. The semiconductor integrated-circuit device according to claim 3, further comprising analog circuits, wherein, among all said analog circuits, a MOSFET circuit constituting a current source is formed using said enhancement-type MOSFETs with high threshold voltage, and a differential MOSFET circuit and a cascade-connected circuit are formed using said enhancement-type MOSFETs with high threshold voltage.

7. The semiconductor integrated-circuit device according to claim 1, wherein, in a standby state in which no signal processing is performed through a signal transferring path, said deletion-type MOSFETs have substrate bias voltage applied in a direction of decreasing

a source-to-drain current decreases.

8. A method for speeding up CMOS circuit operation, comprising:

a first step of designing a signal-processing circuit using enhancement type MOSFETs, said signal-processing circuit comprising a plurality of flip-flop circuits for acquiring and holding signals by use of clock signals, and a plurality of CMOS-constructed logic gate circuits provided between one pair of flip-flop circuits within said plurality of flip-flop circuits;

a second step of extracting, from said plurality of signal transferring paths, a signal transferring path whose signal transferring delay time that exceeds a permissible signal transferring delay time; and

a third step of replacing, among said plurality of logic gate circuits constituting said signal transferring path that has extracted, a logic gate circuit having a delay time longer than said permissible signal transferring delay time when the logic gate circuit is constituted by an enhancement-type MOSFET with a depletion-type MOSFET so that said signal transferring path may provide a signal transferring delay time equal to or less than said permissible signal transferring delay time.

9. The CMOS circuit operational speeding-up method according to claim 8, wherein said third step is followed

by said second step after, of all said enhancement-type MOSFETs constituting said signal transferring paths, a MOSFET having a maximum delay time has been replaced with the depletion-type MOSFET.

10. The CMOS circuit operational speeding-up method according to claim 9, wherein, if said signal transferring path to be extracted is absent, all the delay times of said plurality of signal transferring paths are judged to be equal to or less than said permissible signal transferring delay time.

11. The CMOS circuit operational speeding-up method according to claim 10, wherein, when, in said third step, all MOSFETs of said signal transferring paths are said depletion-type MOSFETs and the signal transferring delay time thereof is taken as a first time, processing returns to said first step and said permissible signal transferring delay time is set as said first time.

12. The CMOS circuit operational speeding-up method according to claim 8, in which, in said third step, among said plurality of logic gate circuits constituting said signal transferring path that has extracted, a logic gate circuit having a delay time longer than said permissible signal transferring delay time when the logic gate circuit is constituted by an enhancement-type MOSFET is replaced with second enhancement-type MOSFETs smaller than said

enhancement-type MOSFETs in terms of threshold voltage so that said signal transferring path extracted may provide a signal transferring delay time equal to, or less than, said permissible signal transferring delay time.

13. The CMOS circuit operational speeding-up method according to claim 8, wherein the signal-processing circuit in said first step is one mounted on an existing semiconductor integrated-circuit device.

14. A semiconductor integrated-circuit device, comprising:

one or more logic gates between an output of a first flip-flop and an input of a second flip-flop;

wherein part of said plurality of logic gates is constituted by a depletion-type MOSFET.

15. A semiconductor integrated-circuit device, wherein:

a signal input block of a first combination circuit and that of a second combination circuit are connected across an output of a first flip-flop;

a signal input block of a third combination circuit is connected to the signal input blocks of said first and second combination circuits;

an input of a second flip-flop is connected to the signal output block of said third combination circuit;

said first, second, and third combination circuits

are constituted by one or more logic gates; and

part of said logic gates is constituted by a depletion-type MOSFET.

16. The semiconductor integrated-circuit device according to claim 14, wherein the logic gates in said semiconductor integrated circuits are further formed with first MOSFETs of the enhancement type whose threshold voltage is a first threshold voltage, and second MOSFETs of the enhancement type whose threshold voltage is a second threshold voltage, said first threshold voltage being higher than said second threshold voltage.

17. The semiconductor integrated-circuit device according to claim 16, further comprising input/output circuits for exchanging signals with external terminals, wherein said input/output circuits are constituted by a plurality of MOSFETs having said first threshold voltage, and said plurality of MOSFETs are MOSFETs different in withstand voltage.

18. The semiconductor integrated-circuit device according to claim 16, further comprising a memory circuit, wherein a memory array of said memory circuit is constituted by enhancement-type MOSFETs of said first threshold voltage, and a peripheral circuit of said memory circuit are constituted by an enhancement-type MOSFET of said second threshold voltage.

19. The semiconductor integrated-circuit device according to claim 16, further comprising analog circuits, wherein among said analog circuits, a MOSFET circuit constituting a current source is formed using enhancement-type MOSFETs of said first threshold voltage, and a differential MOSFET circuit and a cascade-connected circuit are formed using said enhancement-type MOSFETs of said second threshold voltage.

20. The semiconductor integrated-circuit device according to claim 14, wherein, in a standby state in which no signal processing is performed through a signal transferring path, said deletion-type MOSFETs have substrate bias voltage applied in a direction of decreasing a source-to-drain current decreases.